Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously presented) A method for manufacturing a semiconductor device comprising the steps of:

(a) forming a wiring layer on a semiconductor substrate having an integrated circuit and a pad electrically connected to the integrated circuit, the wiring layer being electrically connected to the pad;

(b) forming a resin layer covering the wiring layer;

(c) forming a first concave portion at an area of the resin layer, the area overlapping the wiring layer, by a first process, the first process comprising an exposure step wherein a portion of the resin layer is irradiated with a dose of radiation to form a region with increased solubility and a development step wherein a portion of the region with increased solubility is removed to form the concave portion;

(d) forming a through-hole in the resin layer by removing a bottom of the first concave portion by a second process, the second process differing from the first process, and forming a second concave portion in the wiring layer in such a way that an angle between an osculating plane at any point of a surface of the second concave portion and a top surface of the wiring layer, with the angle being defined outside the second concave portion is 90° or more; and

(e) providing an external terminal in the second concave portion of the wiring layer.

2. (Original) The method for manufacturing the semiconductor device according to claim 1, wherein, in step (c), the first concave portion is formed in such a way that an angle between an osculating plane at any point of a surface of the first concave portion and a top surface of the resin layer, the angle being defined outside the first concave portion, is 90° or more.

3. (Original) The method for manufacturing the semiconductor device according to claim 1 or claim 2, wherein, in step (b), the resin layer is formed of a thermosetting resin precursor and,

prior to step (d), the thermosetting resin precursor is heated.

4. (Currently amended) The method for manufacturing the semiconductor device according to ~~anyone of claims 1 to 3~~ claim 1, wherein the resin layer is formed of a resin precursor that is sensitive to radiation, and

the first process includes irradiation with the radiation and development of the resin precursor.

5. (Currently amended) The method for manufacturing the semiconductor device according to ~~anyone of claims 1 to 4~~ claim 1, wherein the second process comprises dry etching.

6. (Currently amended) The method for manufacturing the semiconductor device according to ~~anyone of claims 1 to 5~~ claim 1, wherein the resin layer is formed of a solder resist.

7. (Currently amended) The method for manufacturing the semiconductor device according to ~~anyone of claims 1 to 6~~ claim 1, wherein the first concave portion has a curved outline at a cross section taken along a plane perpendicular to a top surface of the resin layer.

8. (Currently amended) The method for manufacturing the semiconductor device according to ~~anyone of claims 1 to 7~~ claim 1, wherein the second concave portion has a curved outline at a cross section taken along a plane perpendicular to a top surface of the wiring layer.

9. (Currently amended) The method for manufacturing the semiconductor device according to ~~anyone of claims 1 to 8~~ claim 1, wherein the first concave portion has a width that decreases with depth.

10. (Currently amended) The method for manufacturing the semiconductor device according to ~~anyone of claims 1 to 9~~ claim 1, wherein the second concave portion has a width that decreases with depth.

11. (Currently amended) The method for manufacturing the semiconductor device according to ~~anyone of claims 1 to 10~~ claim 1, wherein the second concave portion is formed in such a way that an opening thereof is entirely disposed inside the through-hole.

12. (Previously presented) A semiconductor device comprising:

a semiconductor chip having an integrated circuit and a pad electrically connected to the integrated circuit;

a wiring layer electrically connected to the pad and

having a concave portion, the concave portion being formed in such a way that an angle between an osculating plane at any point of a surface of the concave portion and a top surface of the wiring layer, the angle being defined outside the concave portion, is 90° or more;

an external terminal joined to the concave portion of the wiring layer; and

a resin layer provided on the wiring layer, the resin layer having a through-hole, the through-hole and the concave portion overlapping each other, the concave portion being formed by an exposure step wherein a portion of the resin layer is irradiated with a dose of radiation to form a region with increased solubility and a development step wherein a portion of the region with increased solubility is removed to form the concave portion.

13. (Original) The semiconductor device according to claim 12, wherein the concave portion has a curved outline at a cross section taken along a plane perpendicular to a top surface of the wiring layer.

14. (Original) The semiconductor device according to claim 12 or claim 13, wherein the concave portion has a width that decreases with depth.

15. (Currently amended) The semiconductor device according to ~~anyone of claims 1 to 14~~ claim 12, wherein the concave portion is formed in such a way that an opening thereof is entirely disposed inside the through-hole.

16. (Currently amended) The semiconductor device according to ~~anyone of claims 1 to 15~~ claim 12, wherein the external terminal contacts the through-hole in the resin layer.

17. (Currently amended) The semiconductor device according to ~~anyone of claims 1 to 16~~ claim 12, further comprising:

a stress relief layer formed on or above the semiconductor chip,

wherein the wiring layer is formed on or above the stress relief layer.

18. (Currently amended) The semiconductor device according to ~~anyone of claims 1 to 17~~ claim 12, wherein the resin layer is formed of a solder resist.

19. (Currently amended) A circuit board including the semiconductor device according to ~~anyone of claims 1 to 18~~ claim 12.

20. (Currently amended) An electronic instrument including the semiconductor device according to ~~anyone of claims 1 to 18~~ claim 12.

21. (Previously presented) A semiconductor wafer comprising:

a semiconductor substrate having a plurality of integrated circuits and pads electrically connected to the plurality of integrated circuits;

a wiring layer electrically connected to the pads and having concave portions, the concave portions being formed in such a way that an angle between an osculating plane at any point of a surface of each of the concave portions and a top surface of the wiring layer, the angle being defined outside each of the concave portions, is 90° or more;

external terminals joined to the concave portions in the wiring layer; and

a resin layer provided on the wiring layer, the resin layer having through holes, the through holes and the concave portions overlapping each other, the concave portions being formed by an exposure step wherein a portion of the resin layer is irradiated with a dose of radiation to form a region with increased solubility and a development step wherein a portion of the region with increased solubility is removed to form the concave portions.

22. (Original) The semiconductor wafer according to claim 21, wherein

each of the concave portions has a curved outline at a cross section taken along a plane perpendicular to a top surface of the wiring layer.

23. (Original) The semiconductor wafer according to claim 21 or claim 22, wherein each of the concave portions has a width that decreases with depth.

24. (Currently amended) The semiconductor wafer according to ~~anyone of claims 1 to 23~~ claim 21, wherein the concave portions are formed in such a way that openings thereof are entirely disposed inside the through holes.

25. (Currently amended) The semiconductor wafer according to ~~anyone of claims 1 to 24~~ claim 21, wherein the external terminals contact the through holes in the resin layer.

26. (Currently amended) The semiconductor wafer according to ~~anyone of claims 1 to 25~~ claim 21, further comprising:

a stress relief layer formed on or above the semiconductor substrate,

wherein the wiring layer is formed on or above the stress relief layer.

27. (Currently amended) The semiconductor wafer according to ~~anyone of claims 1 to 26~~ claim 21, wherein the resin layer is formed of a solder resist.

28. (Previously presented) The method for manufacturing the semiconductor device according to claim 1, wherein, during the exposure step of the first process, the resin layer is irradiated with a sufficient dose of radiation that reaches a part of the resin layer in contact with the wiring layer so as to form the region with increased solubility.

29. (Previously presented) The method for manufacturing the semiconductor device according to claim 1, wherein the region with increased solubility comprises straight walls.

30. (Previously presented) The method for manufacturing the semiconductor device according to claim 1, wherein, during the development step of the first process, a developer is supplied to the region with increased solubility to penetrate the surface of the resin layer to a depth that gradually decreases from a center portion of the region with increased solubility to an edge portion of the region with

increased solubility to thereby form the first concave portions with a concave contour.